HEAT TRANSFER IN THE COOLER - CPU INTERFACE

Pătuleanu Liliana[1], Andronic Florin[2], Manolache-Rusu Ioan-Cozmin[3], Radion Ivan[4]

[1,2,3]*A Department of Mechanical Engineering, Stefan cel Mare University of Suceava, 13 University Street, zip code:720229 Suceava, Romania, [1]lilianapatuleanu@yahoo.com, [2]foiand@yahoo.com, [3]cozmin.manolache@yahoo.com, rad_ivan2005@yahoo.com*

Abstract: *The increased number of requests regarding the cooling of the computers and the miniaturization of electronic components, determined the search for new solutions for intensifying the heat exchange between the processor and the heat sink, the link between these two being realized by means of a thermoconducting paste.*

The current article aims to realize a brief presentation of the concerns regarding the improvement of heat exchange in the CPU – heat sink interface. In the second part, it is realized a calculation method of thermal transfer through TIM, highlighting the presence of some inhomogeneities and gaps in TIM, determining a rise of temperature. The model is used and validated by comparison with numerical results obtained by authors in specialized literature.

Keywords: *heat transfer, cooler, Thermal Interface Material (TIM).*

1. Introduction

The reach of high levels of performance in computer science from the last period, corresponding to the requests imposed by users, has been made possible only by applying technical solutions, which, using an efficient heat transfer, satisfy the high cooling needs.

The first cooling systems were the ones using air and are still frequently applied for microelectric components with reduced thermal charge densities.

For these systems, it is analyzed the thermal performance of the CPU – heat sink package, also including here the Thermal Interface Material, next referred to shortly as TIM. It is justified the interest of manufacturers and users of these systems, due to the way thermal connections of the two components are realized: by means of thermal paste as heat exchange environment.

1.1. Considerations regarding the use of TIM as cooler – CPU interface

1.2. Models of assembly CPU – heat sink

The heat exchange between the heat sink and the CPU core is realized using the thermal transfer material, inserted between solid surface layers. In the absence of this material, the contact surface is reduced because of the irregularities in the material. Between the heat sink and the core there are small air bubbles that are bad heat exchangers and must be filled with a specific material. By applying TIMs to the materials, having a much higher thermal conductivity, "are exceeded the limits created by the existence of gaps that appear as a result of irregular deposits, surface roughnesses, defects and interface alignment". Therefore, it is very important how the assembly of the components is realized, in order to prevent the appearance of gaps that reduce thermal performances and the reliability of the package.

Taking into account the continuous increasing cooling capacity, which should be ensured by the cooling systems, the designers and manufacturers were concerned regarding the architecture of the thermal package. They proposed technical solutions of positioning the components for maximum efficiency. Mahajan and others, in [2], present two "thermal architectures": the first model in which the heat sink is applied at the backside of the silicon chip using a TIM-1 material, designed for small spaces (for example, laptops); the second model with a heat spreader integrated between the chip and the heat sink by inserting TIM-1 materials, respectively TIM-2, architecture used for desktops and servers.

Wei analyzes, in [3], the same thermal design "with two levels" for high performance servers. It is analyzed the thermal conductivity and heat

dissipation of a metallic material with a high thermal conductivity. The attention is drawn to the right choice of TIM and, from the point of view of the thermal dilatation coefficient, that must be close to the coefficient of the silicon chip, in order to maintain for a long time a high thermal performance and the reliability of the package.

1.3. Materials used in thermal transfer

It is considered, in [4], that an "ideal TIM" must meet the following requirements: high thermal conductivity; to be easily deformed with low contact pressures; to have low thickness; to be without surface leaks; to be reliable; not to be toxic; to be easily applied and cleaned.

Other requests refer to applicability. The heat sink should be easily removed and TIM should be easily cleaned, so that the cooling system can be remade.

Nowadays, there are used multiple types of TIMs: *Phase Change (Thermal Pads)*,which deposits in the form of an adhesive band of thermal transfer that melts at 55ºC; *Thermal Grease*, which ensures a very low thermal resistance, but dries in time and, as a result, thermal transfer becomes difficult; *Thermal compound* is a better thermal transfer paste because it becomes liquid and fills the air bubbles, but it has the disadvantage of, above a certain temperature, the paste becomes like rubber; fibers covered with silicon, epoxy materials, graphite, aluminum strips.

Graphene composite and multi-layer graphene is a new material realized in USA, [4], with exceptional properties because pure grapheme has a thermal conductivity higher than diamond, the best heat conductor known.

Wei studied, in [3], the thermal performances of a metallic TIM, the composite In-10Ag, and compared with the properties of other TIMs, proving its qualities.

At University of Suceava, there were carried out tests, presented in [12], to see the behavior of *Thermal Grease* when heated. There were highlighted the following: the appearance of micro and nanochannels in the fresh applied paste; the phenomenon of material dilatation that leads to the "pump up" effect of the material situated inside CPU – cooler; small variations of roughness values.

1.4. Calculation models for thermal parameters of TIM

TIMs are used for minimizing thermal contact resistance, which depends mainly on the thermal conductivity of the material and the thickness of the layer.

For increasing the value of the maximum dissipated power, there was paid extra attention to reducing the thermal resistance at the interface and reducing the value of its two components: TIM resistance of the entire structure expressed as a ratio between BLT (the thickness of the link line) and k_{TIM} (thermal conductivity of TIM); contact resistance TIM – CPU, respectively TIM – heat sink, [2]. There were analyzed the ways of reducing the thermal resistance by: reducing BLT, increasing the thermal conductivity and reducing the contact resistances.

There were realized:

- The calculation model for thermal conductivity of TIMs considered a "polymeric matrix", in [5], loaded with solid particles, as a function of the following form:

$$k_{TIM} = f(k_f, k_m, \phi, R_b) \quad (1)$$

where: k_f is the thermal conductivity of the fill material, k_m is the thermal conductivity of the silicon oil, ϕ is the volume fraction and Rb is the contact resistance between the particles and the polymeric matrix;

- The empiric model for BLT, in [6], in the case of particles loaded with polymeric materials in TIM. After the experimental analysis of the materials, they proposed the following relation for BLT:

$$BLT = 1{,}31 \cdot 10^{-4} \left(\frac{\tau_y}{P} \right)^{0{,}166} \quad (2)$$

where: τ_y is the efficiency of TIM and P is the applied pressure.

- The calculation model for the resistance of contact between a silicon device and a heat sink with a layer of TIM measuring a thickness t, in [7], as follows:

$$R_{Total} = t/(k_{Silicon} \cdot A) + R_{Contact} + t/(k_{TIM} \cdot A) + t/(k_{Aluminiu} \cdot A) \quad (3)$$

In the same paper it is studied the variation of thermal resistance according to t.

- The calculation model for thermal resistance taking into account the roughness of the surfaces,

in [8], the general common conductance is given by the relation:

$$\frac{1}{h_j} = \frac{1}{\left(h_{j,1}\right)} + \frac{t}{k} + \frac{1}{\left(h_{j,2}\right)} \qquad (4)$$

The model was applied at different contact pressure, showing higher values of thermal resistance for air, compared to helium or thermal paste.

- The calculation model from [5], for the sum of contact resistances of TIMs:

$$R_{C_{1+2}} = \left(\frac{\sigma_1 + \sigma_2}{2k_{TIM}}\right) \cdot \left(\frac{A_{nominal}}{A_{real}}\right) \qquad (5)$$

where: σ_1 and σ_2 are the roughnesses of the surface sublayers; $A_{nominal}$ is the nominal surface; A_{real} is the real heat transfer area, which is lower than the nominal surface, because of the air from the gaps on the surface sublayers.The calculation model of the thermal resistance of TIM, in [9], is:

$$\Theta_{TIM} = \frac{1}{A} \cdot \left(\frac{t}{K} + \Theta_{INT1} + \Theta_{INT2}\right) = \frac{1}{A} \cdot \left(\frac{t}{K} + \Theta_{INT}\right) \qquad (6)$$

where: A is the cross - sectional area of TIM, t is the thickness of the line of BLT, K is the thermal conductivity for the block, Θ_{INT1} and Θ_{INT2} are the values of thermal resistance on each side, for the surface unit; Θ_{INT} is the thermal resistance for both sides.

In order to increase the value of the maximum dissipated power, it is necessary for the total thermal resistance to be reduced.

1.5. Analysis of the TIN layer

The structure of the TIM situated in cross-section was analyzed SEM by Schacht, in [1]. It was observed that pores appear at the boundary surface between the silicon chip and Ag particles, gaps filled with adhesive – copolymer TIM.

Wei investigates, in [3], into the impact of the gaps presented in TIM, with consequences regarding the increase of joint temperature.

Sery, in [11] and Wei, in [3], signal the presence of "hot-spots" on the surface of the CPU, in which the power density could be three to eight times higher than the medium power density, [3]. It is justified, in this way, the concern for "hot-spots" elimination from the cooling package.

By using an atomic force microscope AFM-universal, Mihai scanned the interface layer of different CPUs and highlighted the flow microchannels, measuring a width of approximately 2μm and a height of 2000 A, [13].

Mahajan, in [2], studied the reliability of the thermal paste used as a heat transfer environment. It was applied an accelerated testing method for evaluating the degradation of the interface, as a result of the evacuation of grease by pumping.

3. Calculations regarding heat transfer through TIM

We propose to analyze the transfer of heat provided by a CPU dissipating a power of 95 W, through a TIM and to the radiator, in case of forced air cooling on only one side of the CPU.

It is applied the calculation model proposed in [12, 14] and developed in [15, 16]. The heat transfer is bidirectional: the heat flux $\dot{q}_1$ to the heat sink by using a TIM; the heat flux $\dot{q}_2$ to the sublayer and mainboard.

The behavior of the heat sinks when transmitting heat can be investigated using analytical methods or finite element analysis. It is presented the finite element analysis developed, in [15], in order to determine the temperature field for a CPU cooling system.

The differential equation of temperature, Fourier equation has the following form:

$$\frac{\partial T}{\partial \tau} = \alpha \nabla_T^2 + \frac{q_v}{\rho c_p} \qquad (7)$$

where: T[K] is the temperature, τ[s] is the time, $q_v = q_v(x,y,z,\tau)[W/m^3]$ represents power densitygenerated by the CPU, $\alpha[m^2/s]$ is the thermal diffusivity, $\rho[kg/m^3]$ is thedensity, c_p[J/kg K] is the specific heat of the material at constant pressure.

The temperature distribution in the wall is obtained using the model from [14], by integrating equation (7) for a stationary and unidirectional regime, of the following form:

$$T_{(x)} = -q_v \frac{x^2}{2k} + \left(\frac{T_{s,2} - T_{s,1}}{2\delta} + \frac{q_v \delta}{k}\right) \cdot x + T_{s,1} \quad [K] \qquad (8)$$

in which: $T_{s,1}$, $T_{s,2}$, [K] represent the temperature of the exterior sides of the wallat x = 0, respectively at x = 2δ; k [W/m·K] is the conductive heat transfer; x[m] is the distance from the maximum temperature, corresponding to the internal heat source, to the fringe of the cooling system; δ[m] is the characteristic length in x direction.

The maximum temperature Tmax in the wall is reached for x = x_m, which results from the following condition:

$$x_m = \delta + \frac{k}{q_v} \cdot \frac{T_{s,2} - T_{s,1}}{2\delta} \qquad [m] \tag{9}$$

By replacing x = x_m in equation (8) the maximum temperature $T_{max}[K]$ in the wall is:

$$T_{\max} = \frac{q_v \cdot \delta^2}{2k} + \frac{k}{8 \cdot q_v \cdot \delta^2}\left(T_{s,2} - T_{s,1}\right)^2 + \frac{T_{s,1} + T_{s,2}}{2} \tag{10}$$

There are imposed boundary conditions of the third type, from [14]:

- If x = 0, $-k\left.\frac{dT}{dx}\right|_{x=0} = -h_1\left(T_{s,1} - T_{\infty,1}\right)$ (11)
- If x = 2δ, $-k\left.\frac{dT}{dx}\right|_{x=2\delta} = h_2\left(T_{s,2} - T_{\infty,2}\right)$ (12)

The temperatures of the wall surfaces $T_{s,1}$, $T_{s,2}$ [K] are determined as follows:

$$T_{s,1} = T_{\infty,1} + \frac{T_{\infty,2} - T_{\infty,1} + 2 \cdot \delta \cdot q_v \left(\frac{1}{h_2} + \frac{\delta}{k}\right)}{1 + \frac{h_1}{h_2} + 2\frac{h_1}{k}\delta} \tag{13}$$

$$T_{s,2} = T_{\infty,2} + \frac{T_{\infty,1} - T_{\infty,2} + 2\delta \cdot q_v \left(\frac{1}{h_1} + \frac{\delta}{k}\right)}{1 + \frac{h_2}{h_1} + 2\frac{h_2}{k}\delta} \tag{14}$$

in which $T_{\infty,1}$, $T_{\infty,2}$ represent the temperatures of the cooling agents.

The Eq. 13,14 are valid in all directions, considering the small dimensions of the areas adjacent to the CPU. In order to determine the temperature field, Eq. 13 and 14 are applied in all the three directions, using a distribution matrix, in a network [$x_i \cdot y_j$].

The graphical representations indicate the variations of temperature inside the solid in the xy plane, Fig. 1, and in the surroundings of the CPU core, Fig.2.

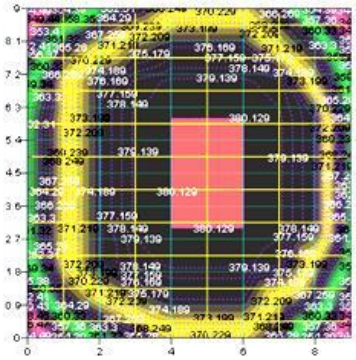

Figure 1. *The Txy isotherms.*

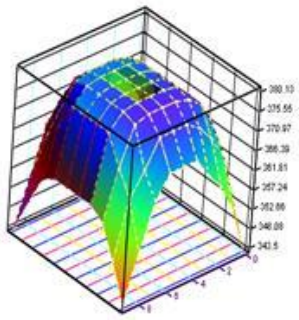

Figure 2. *The temperature field Txy.*

It is observed that the maximum temperature of 380,129 K is recorded at the surface of the CPU, and the lowest values of 343,500 K in the furthest points from the core, correspond to the TIM layer and to the heat sink base.

In order to bring forward the effect of the irregularities from the TIM layer on the heat exchange and CPU temperature, it is applied the analytical model presented previously in MathCAD. In the case in which the material of the interface has irregularities, the heat conduction coefficient modifies because there appear small areas in which air is retained and blocks the efficient heat transmission.

There were calculated values of temperatures in z direction, in two cases: Tz1 when TIM layer is homogeneous, Fig. 3, 4 and Tz2 in the second situation, in which, the thermal transfer material is inhomogeneous, Fig. 5, 6.

By analyzing the obtained values, it is discovered am accentuated increase of temperatures Tz in areas with irregularities, which is also shown in the graphical representations of the temperature field from Fig. 3, 4, 5, 6.

Homogeneous TIM

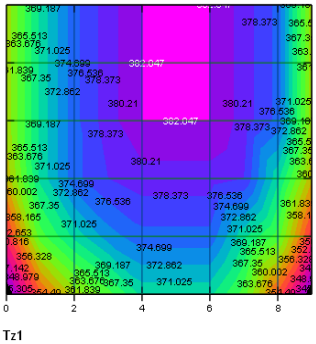

Figure 3. *Isotherms Tz1.*

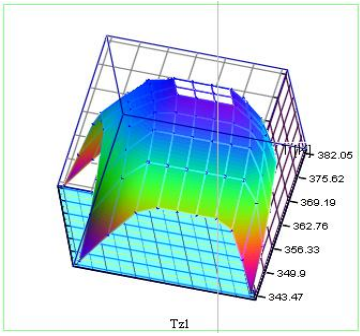

Figure 4. *The temperature field Tz1.*

Inhomogeneous TIM

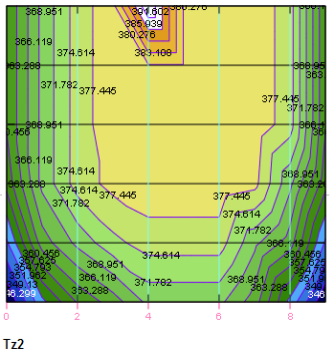

Figure 5. *Isotherms Tz2.*

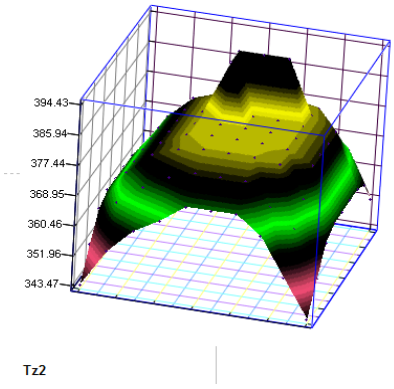

Figure 6. The temperature field Tz2.

The Figures 3, 5 show the temperature variation in case of a homogeneous material of the CPU interface, with the same thermal properties and with constant heatconduction coefficient in the entire volume.

The Figures 4, 6 represent a calculation simulation of the effect of some "defects" in TIM, case in which, the heat conduction coefficient modifies and produces a significant increase of Tz temperature, which can greatly affect the integrity of the processor.

4. Conclusions

The presented calculation model allows the calculation of the temperature values and the discovery of the maximum values in areas with irregularities, where the power density becomes concentrated and dangerous.

In the case when deviations from a presumably normal level of temperature values are high, it is imposed to adopt new assembly solutions of the package chip – processor or changing the TIM material.

The obtained results were compared with the ones obtained in the specialized literature. The representations from Fig. 3, 4, 5, 6 show that the temperatures have the same values, the same way of variation as the ones obtained by authors in [3, 12,16]. Therefore, the results are validated.

ACKNOWLEDGMENT

This paper was supported by the project "Improvement of the doctoral studies quality in engineering science for development of the knowledge based society-QDOC" contract no. POSDRU/107/1.5/S/78534, project co-funded by the European Social Fund through the Sectorial Operational Program Human Resources 2007-2013.

References

[1] Schacht, R., D May, B Wunderle, Wittler, O., Gollhardt, A., B. Michel and H. Reichl, *Characterization of Thermal Interface Materials to Support Thermal Simulation*, http://arxiv.org/abs/0709.1849, Proceedings of 12th International Workshop on Thermal Investigations of ICs - THERMINIC 2006, Nice - France, 2006.

[2] Mahajan, R., CP. Chiu, and R. Prasher,*Thermal Interface Materials: A Brief Review of Design Characteristics and Materials*, Electronics Cooling - 2004.

[3] Wei, J., *Challenges in Cooling Design of CPU Packages for High-Performance Servers*, Heat Transfer Engineering, 29(2): 178-187, 2008.

[4]San José *Thermal Interface Materials*, [Interactiv] http://www.engr.sjsu.edu/ndejong/ME%20146%20files/Thermal%20Interface%20Materials.ppt. - 2012.

[5]Prasher R., Shipley, J., Prstic, S., Koning, P., and Wang, J-L., *Thermal Resistance of Particle Laden Polymeric Thermal Interface Materials*, Journal of Heat Transfer, Vol. 125, 2003.

[6]Prasher R., *Surface Chemistry and Characteristics Based Model for Thermal Contact Resistance of Fluidic Interstitial Thermal Interface Materials*, Journal of Heat Transfer, 2001.

[7] Blazej, D., *Thermal Interface Materials* Electronics Cooling, 2003.

[8]Teertstra P., Yovanovich, M.M., şi Culham, J.R., *Analytical Forced Convection Modeling of Plate Fin Heat Sinks* [Conferinţă] / Proceedings of 15th IEEE Semi-Therm Symposium, 1999.

[9] Guenin, B., *Packaging Challenges For High Heat Flux Devices*, Electronics Cooling, 2006.

[10] Guenin, B., *Calculations for Thermal Interface Materials*, Electronics Cooling, 2003.

[11] Sery, D., *Life IsCMOS:WhyChase the Life After*" in Proc. Design Automation Conf., New Orleans, Louisiana, USA, pp. 78-83, 2002.

[12] Mihai, I., Pîrghie, C., Zegrean, C., *Research Regarding Heat Exchange Through Nanometric Polysynthetic Thermal Compound to Cooler–CPU*, Heat Transfer Engineering. 2010. Vol. 31.

[13]Mihai, I., *Heat Transfer in Minichannels and Microchannels CPU Cooling Systems* InTechOpen, www.intechopen.com, p.64-68, 2011.

[14] Chiriac F., A. Leca, M. Pop, A. Badea, L. Luca, N. Antonescu, D. Peretz, *Processes of heat and mass transfer in the industrial facilities*, Ed. Tehnică, Bucharest, 1982.

[15] Belmiloudi, A., *Heat Transfer/Theoretical Analysis, Experimental Investigations and Industrial Systems, chapter 4, Heat transfer in Minichannels and Microchannels CPU cooling systems* - Viena : INTECH, 2011.

[16] Mihai, I., Suciu, C., Pătuleanu, L., *Modeling of HEAT Transfer in Microchannels of a CPU - Heat Sink Cooling System*, 2012.